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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/718,270 | 11/19/2003 | Shridhar Mukund | ADAPP236 | 9981 |

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| EXAMINER | |
|---|---|
| CHEA, PHILIP J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2153 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/718,270 | MUKUND ET AL. | |
| | Examiner | Art Unit | |
| | PHILIP J. CHEA | 2153 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to an Amendment filed November 28, 2007. Claims 1-20 are currently pending. Any rejection not set forth below has been overcome by the current Amendment.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,8,14 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Amagai et al. (US 7,130,312), herein referred to as Amagai.

As per claim 1, Amagai discloses a method for efficiently processing layers of a data packet, as claimed, comprising:

defining a pipeline of processors in communication with a distributed network and a central processing unit (CPU) of a host system (see Fig. 7, where three processes are performed simultaneously);

receiving a data packet from the distributed network into a first stage of the pipeline of processors (see column 12, lines 21-26, where layer processing portions are considered the pipeline of processors);

transmitting the processed data packet to a second stage for processing associated with the second stage (see column 6, lines 27-37, where the stages are considered when the packet travels through different layer processing portions);

repeating the operations of processing the data packet and transmitting the processed data packet for successive stages (see Fig. 7, where X,Y,Z, are layered (stages) processing portions repeating operations for different packets); and

transmitting the data packet from the final stage to the CPU of the host system (see Fig. 2, where the processor (higher layer) finally receives the data).

Although the system disclosed by Amagai shows substantial features of the claimed invention (discussed above), it fails to expressly disclose processing the data packet to remove a header associated with the first stage; and repeating the operations until a header associated with a final stage has been removed from the data packet.

However, Amagai does disclose processing header portions of packets according to the different layers such as layer 3 and layer 4 (see column 12, lines 61-64) and also that a packet header can be updated, converted, deleted and added (see column 5, lines 13-20). At the time of the invention, a person having ordinary skill in the art would have found it obvious (if not implied) for each layer to remove their corresponding header while the data flows up the OSI model until it is converted back to data and presented to the user. Therefore, the headers would have been removed as the packet traveled through each stage of the pipelined processors.

As per claims 2,9, Amagai further discloses that the packet is an Ethernet packet (see Fig. 4A).

As per claims 3,12,17, Amagai further discloses each of the processors of the pipeline of the pipeline of processors includes at least three buffers configured to maintain a line rate (see Fig. 6).

As per claim 4, Amagai further discloses that the successive stages corresponds the layers of the data packet (see Fig. 7, where X,Y,Z, are layered (stages) processing portions repeating operations for different packets).

As per claims 5,10,16, Amagai further discloses that the layers are selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer (see column 12, lines 61-64).

As per claims 8,11,14, Amagai discloses a central processing unit (CPU);

a network interface card (NIC) configured to process data packets, the NIC including (see Fig. 1),

a plurality of processors arranged in pipeline architecture, the plurality of processors defining a receiving pipeline and a transmitting pipeline (see Fig. 7 and Fig. 2), each of the plurality of processors associated with a pipeline stage, each pipeline stage configured to process a header associated with the data packets (see column 6, lines 27-37, where the stages are considered when the packet travels through different layer processing portions), wherein the receiving pipeline removes headers from the data packets and the transmitting pipeline adds headers to the data packets (see

discussion above regarding the packet traveling up the OSI model and column 5, lines 13-27, showing a packet header can be deleted and added).

As per claim 15, Amagai further discloses that the pipeline stage is associated with a layer of a header of the data packets (see column 12, lines 15-26 and lines 61-64).

3. Claims 6,7,13,18,19,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amagai as applied to claims 1,8,14 above, and further in view of Chandra et al. (US 7,185,153), herein referred to as Chandra.

As per claim 6, Amagai shows defining instructions for processing the data packet (see Fig. 7, where X,Y,Z, are layered (stages) processing portions repeating operations for different packets).

Although the system disclosed by Amagai shows substantial features of the claimed invention (discussed above), it fails to disclose enabling an arithmetic logic unit (ALU) associated with each processor to process the instructions.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Amagai, as evidenced by Chandra.

In an analogous art, Chandra discloses the processing of packets (see Fig. 4A), using an ALU to process the instructions (see column 7, lines 23-30).

Given the teaching of Chandra, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Amagai by employing an ALU, such as disclosed by Chandra, in order to process instructions from multiple threads.

As per claims 7,13,18, Amagai in view of Chandra further disclose aligning the instructions by a least significant bit; and executing each of the instructions to a defined bit size (see Chandra column 2, lines 10-19).

As per claim 19, Amagai in view of Chandra further disclose that each of the processors are configured to execute a two stage pipeline process (see Chandra column 2, lines 30-37).

As per claim 20, Amagai in view of Chandra further disclose that the data packets have a variable packet size (see Chandra column 2, lines 20-29).

***Response to Arguments***

4. Applicant's arguments filed November 28, 2007 have been fully considered but they are not persuasive.

A) Applicant contends that Amagai does not disclose a plurality of pipelined processors.

In considering A), the Examiner respectfully disagrees. Amagai discloses separate processing portions, which the Examiner considers as the plurality of pipelined processors (see column 6, line 58 - column 7, line 7, *describing the different processing portions and the jobs they perform*). Since each processing portion can perform a different process at the same time another process is performed, the Examiner believes it teaches the plurality of pipelined processors. The timing sequence of Fig. 7 shows three separate processes being executed by the separate processing portions (e.g. process for reception of a packet, layer 2 reception processing and layer 3 processing portion) at the same time. That is, a three processor pipeline architecture, processing 3 different packets simultaneously (see column 12, lines 15-33). The Examiner invites the Applicant to clearly claim that the pipeline processing architecture is explicitly performed by a plurality of separate processors that are not located on a single chip in order to possibly overcome the prior art rejection.

***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHILIP J. CHEA whose telephone number is (571)272-3951. The examiner can normally be reached on M-F 6:30-4:00 (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Philip J Chea
Examiner
Art Unit 2153

PJC 2/26/08
/Glenton Burgess/
Supervisory Patent Examiner, Art Unit 2153